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Application / Conf. No.	09/510,203 / 2126
Filing Date	February 22, 2000
First Named Inventor	Carol A. Fields
Examiner Name	Ayal I. Sharon
Art Unit	2123
Patent No.	
Attorney Docket Number	X-560 US

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
- [ ] Amendment / Reply
  - [ ] Preliminary Amendment
  - [ ] After Final
  - [ ] Affidavit(s)/declaration(s)
- [ ] Extension of Time Request
- [ ] Change Status to LARGE ENTITY
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A)
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers (with Recordation Cover Sheet)
- [ ] Declaration / Oath
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition -
- [ ] To Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] After Allowance Communication to
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Status Letter
- [X] Return Receipt Postcard
- [ ] Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Customer Number Attn:	Justin Liu	24309 *(Customer Number)*	Reg. Number 51,959
Signature			
Date	April 23, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number:	24-0040

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on this date: April 23, 2004

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This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to botain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.**

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FEE TRANSMITTAL for FY 2003

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TOTAL AMOUNT OF PAYMENT	($) 330.00

Complete if Known	
Application / Conf. No.	09/510,203 / 2126
Filing Date	February 22, 2000
First Named Inventor	Carol A. Fields
Examiner Name	Ayal I. Sha[illegible]
Art Unit	2123
Attorney Docket No.	X-560 US

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees, any additional fees required, and credit any over payments to:

[X] Deposit Account

Deposit Account Number: 24-0040

Deposit Account Name: XILINX, INC.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
1001	770	Utility filing fee	
1002	330	Design filing fee	
1003	510	Plant filing fee	
1004	770	Reissue filing fee	
105	160	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Indep. Claims		- 3** =		X		=	
Multiple Dependent Claims				X		=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Fee ($)	Fee Description
1202	18	Claims in excess of 20
1201	86	Independent claims in excess of 3
1203	290	Multiple dependent claim, if not paid
1204	86	**Reissue independent claims over original patent
1205	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
1051	130	Surcharge - late filing fee or oath	
1052	50	Surcharge - late provisional filing fee or cover sheet.	
1812	2,520	For filing a request for exparte reexamination	
1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	Extension for reply within first month	
1252	420	Extension for reply within second month	
1253	950	Extension for reply within third month	
1254	1,480	Extension for reply within fourth month	
1255	2,010	Extension for reply within fifth month	
1401	330	Notice of Appeal	
1402	330	Filing a brief in support of an appeal	$330
1403	290	Request for oral hearing	
1451	1,510	Petition to institute a public use proceeding	
1452	110	Petition to revive - unavoidable	
1453	1,330	Petition to revive - unintentional	
1501	1,330	Utility issue fee (or reissue)	
1460	130	Petitions to the Commissioner	
1807	50	Petitions related to provisional applications	
1806	180	Submission of Information Disclosure Stmt	
8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	Request for Continued Examination (RCE)	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 330.00

SUBMITTED BY

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Signature				Date	04-23-2004

Complete (if applicable)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Carol A. Fields et al.
Assignee:	Xilinx, Inc.
Title:	"SYSTEM AND METHOD FOR ASSISTING IN THE DEVELOPMENT AND INTEGRATION OF REUSABLE CIRCUIT DESIGNS"

Serial No.:	09/510,203	Filing Date:	02/22/2000
Examiner:	Ayal I. SHARON	Art Unit:	2123
Docket No.:	X-560 US	Conf. No.:	2126

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Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. §1.192 for the above-referenced patent application and is being filed in triplicate.

I. Real Party in Interest

The real party in interest is Xilinx, Inc., having a place of business at 2100 Logic Drive, San Jose, California 95124-3400. The above referenced patent application is assigned to Xilinx, Inc.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-19 are presented for appeal. Claims 1-9, 14, and 16-19 stand rejected under 35 USC §102(e) as being anticipated by US patent number 6,223,326 to Fields et al.

("Fields-1"). Claims 1, 9, 11, and 18-19 stand rejected under 35 USC §103(a) over US patent number 5,673,199 to Gentry ("Gentry") in view of the paper entitled, "6.111 Introductory Digital Systems Laboratory" ("Emacs"). Claims 2-3 and 13-14 stand rejected under 35 USC §103(a) over Gentry in view of Emacs and further in view of the Web pages collectively entitled, "Introduction to Synopsys to XACT M1 Design Flow" ("XACT"). Claims 10, 12 and 15 are deemed allowable if amended to include the limitations of the base claim and intervening claims.

The final Office Action dated November 5, 2003 withdrew the rejection of claim 13. However, the Summary sheet of that Action indicated that claim 13 stood rejected. It is respectfully submitted that claim 13 is thought to be allowable over the prior art of record.

The claims presented for appeal may be found in the attached Appendix of Appealed Claims.

IV. Status of Amendments

The application was initially filed on February 22, 2000, including claims 1-19. In reply to a first Office Action, which was mailed on May 19, 2003, a Response was filed on August 12, 2003, and no claims were amended. A final Office Action was mailed on November 5, 2003. A response to the final Office Action was filed on December 22, 2003, and an Advisory Action was issued on January 22, 2004. A Notice of Appeal was filed on February 26, 2004, and an Advisory Action was mailed on March 15, 2004.

V. Summary of Invention

Various embodiments of Appellants' invention are directed to a method and system for developing a reusable electronic

circuit design module and using the design module in a debug mode. In one embodiment, the functional design elements comprising a design module are entered into a database along with documentation elements that describe the design elements (FIG. 1, 102; FIG. 2, 202; page 4, ll. 1-27; p. 7, l. 32; p. 9, ll. 32-35). The functional design elements are linked with selected ones of the documentation elements in the database (FIG. 1, 102; page 4, ll. 1-27; p. 9, ll. 32-35). A testbench is simulated with the design module (FIG. 1, 122; FIG. 3, 314; p. 11, ll. 22-32), and the generated results are stored in a database and linked with the functional design elements (FIG. 1, 118; FIG. 3, 318; p. 11, ll. 22-32). By linking the design elements, documentation, translation results, and simulation results, the characteristics of the design module are easily ascertained by a designer who is reusing the design module (p. 2, ll. 18-21).

In another embodiment, a system includes a database, a design inspector, a debugging-support module, and a functional simulator (FIG. 1; p. 4, l. 34 - p. 7, l. 17). The database is arranged for storage of the design elements and documentation elements (FIG. 1, 102), and the design inspector (FIG. 1, 104) is coupled to the database. The design inspector links the functional design elements with selected ones of the documentation elements (p. 5, l. 17-27). The debugging-support module is coupled to the simulator and to the database, and generates a netlist from the design module, wherein the netlist is suitable for simulation (FIG. 1, 124, 114; p. 5, ll. 5-17). The functional simulator is coupled to the debugging-support module and simulates a testbench with the design module, whereby simulation results are generated (FIG. 1, 122, 118; p. 5, ll. 5-17). The simulation results are entered in the database by the debugging-support module

and thereafter linked with the design elements (FIG. 1, 120; p. 6, ll. 18-33).

VI. Issues for Review

Issue 1: Is the rejection of claims 1-9, 14, and 16-19 under 35 USC §102(e) over Fields-1 (USP #6,223,326) proper when the rejection does not show that Fields-1 teaches or suggests every limitation of the claimed invention?

Issue 2: Is the §103(a) rejection of claims 1, 9, 11, and 18-19 proper when the asserted *Gentry* (USP #5,673,199) and *Emacs* (paper entitled, "6.111 Introductory Digital Systems Laboratory") references fail to teach or suggest every limitation of the claims, when the rejection fails to cite evidence of motivation, and there is no apparent likelihood of successfully combining the references?

Issue 3: Is the §103(a) rejection of claims 2-3 and 14 proper when the asserted *Gentry*, *Emacs*, and *XACT* references fail to teach or suggest every limitation of the claims, when the rejection fails to cite evidence of motivation, and there is no apparent likelihood of successfully combining the references?

VII. Grouping of Claims

For purposes of this appeal, claims 1, 9, 16, 17, 18, and 19 are in group I; claim 2 is in group II; claims 3 and 14 are in group III; claim 4 is in group IV; claim 5 is in group V; claim 6 is in group VI; claims 7 and 8 are in group VII; and claim 11 is in group VIII. The claims as now presented in the different groups do not stand or fall together.

VIII. Argument

Issue 1: The §102(e) rejection of claims 1-9, 14, and 16-19 is not proper when Fields-1 does not teach or suggest every limitation of the claimed invention.

In order to establish a *prima facie* case of anticipation, the Examiner must present a reference that completely corresponds to the claimed invention.

Claims 1, 18, and 19 in group I include limitations of entering the functional design elements into a database; entering documentation elements into the database; linking the functional design elements with selected ones of the documentation elements; simulating a testbench with the design module, whereby simulation results are generated; storing the simulation results in the database; and linking the simulation results with the functional design elements. The rejection fails to show that Fields-1 shows all the limitations.

For example, the rejection alleges that Fields-1 teaches simulating a test bench with the design module, storing the simulation results in the database, and linking the simulation results with the functional design elements. However the cited portions of Fields-1 (FIG. 1, elements 104, 110 and associated text; and FIG. 3, elements 306-318) do not appear to mention storing simulation results in any manner. Nor does the cited text allege storing the simulation results in a database and linking the simulation results with the functional design elements.

The rejection alleges that "storing the simulation results is inherent in Fields-1 [because] the Performance/Density analyzer would not be able to 'provide the results as output' without storing them in RAM or some form of

media." It is respectfully submitted that the inherency allegation is unfounded because it fails to address the limitations that relate to storing the simulations results in a database and linking the simulation results with the functional design elements.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) (MPEP 2112). The rejection fails because no showing has been made that storing simulation results in a database and linking the results to functional design elements necessarily flows from Fields-1's Performance/Density Analyzer.

The present claims include limitations of storing the simulation results in a database, and the Office Action alleges that Fields-1 would need to store performance/analysis results in a RAM or some form of media in order to provide the

results as output. Those skilled in the art will appreciate that storing the results in RAM or media does not necessarily imply storing the data in a database. Furthermore, storing data in a RAM or other media does not imply linking the data to functional design elements in a database. Therefore, the rejection fails to show that these limitations are shown, suggested, or inherent in Fields-1.

The rejection is further improper because it is inconsistent in the selection and application of elements of Fields-1 alleged to correspond to the claim limitations. Recall the claim limitations of simulating a testbench with the design module, whereby simulation results are generated; storing the simulation results in the database; and linking the simulation results with the functional design elements. To show correspondence, the rejection needs to demonstrate that the output from the alleged simulating element of Fields-1 is the output that is stored and linked with the functional design elements. However, the rejection fails to establish this correspondence. The rejection first alleges that the performance density analyzer of Fields-1 corresponds to the claimed simulating, and then alleges that the database of problematic design elements in Fields-1 corresponds to the claimed storage and linking of simulation results. The rejection fails because it does not show that the output from the performance density analyzer of Fields-1 is in any way stored in a database and linked to functional design elements. Instead, the rejection uses the database of problematic coding styles to support the allegation, and no showing is made that the database of Fields-1 contains any data from the performance density analyzer.

For at least the reasons set forth above, the rejection fails to show that claims 1, 18, and 19 of group I are

anticipated, and the rejection should be overruled. Claims 9, 16, and 17, also of group I, are allowable for the reasons set forth above.

Claim 2 of group II includes limitations of translating the functional design elements into a netlist; and linking elements of the netlist with selected ones of the functional design elements. The rejection fails to show that Fields-1 teaches these limitations.

The most recent rejection cites Fields-1, col. 4, ll. 17-37 as teaching these limitations, and specifically alleges that linking the netlist elements with selected ones of the functional design elements is inherent in Fields-1. In view of the requirements to establish inherency, as set forth above, the Office Action fails to provide sufficient evidence. The Office Action has only alleged that commercially available synthesizers analyze netlists for performance and density. The Office Action fails to provide any evidence that linking netlist elements with selected ones of the functional design elements is a necessary condition to performing the alleged analysis. Therefore, the Office Action fails to show that the limitations are inherent in Fields-1 and fails to show that claim 2 is anticipated.

The rejection of claims 3 and 14 in group III is deficient for reasons similar to those set forth above for claim 2. Claims 3 and 14 include limitations of linking elements of the physical implementation with selected ones of the functional design elements. The cited portions of Fields-1 do not appear to show or suggest such linking. Specifically, the rejection cites the converter and database of problematic design elements (FIG. 1, 102 and 108) of Fields-1 as corresponding to these limitations. However, neither of these elements in any apparent manner suggests the linking elements of a physical implementation with functional design elements. It appears that the database 108 of Fields-1 stores problematic design elements, not elements of the physical implementation linked to

functional design elements as claimed. Therefore, the rejection fails to show that claims 3 and 14 are anticipated.

Claim 4 in group IV includes limitations of entering simulation elements in the database; and linking the simulation elements to associated ones of the design elements. The cited portions of Fields-1 do not appear to show or suggest such linking. Specifically, the rejection cites the performance/density analyzer and database of problematic design elements (FIG. 1, 104 and 108) of Fields-1 as corresponding to these limitations. However, neither of these elements in any apparent manner suggest the linking of simulation elements with functional design elements. The database 108 of Fields-1 stores problematic design elements, not simulation elements linked to functional design elements as claimed. Therefore, the rejection fails to show that claim 4 is anticipated.

Claim 5 in group V includes limitations of entering documentation for a design script in the database; and linking the documentation of the design script to the design elements comprising the design module. The most recent rejection alleges that the teaching in Fields-1 of Verilog and VHDL coding teaches the limitations related to design scripts. However, those skilled in the art will understand that Verilog and VHDL are not scripting languages, but are Hardware Description Languages (HDLs). Example scripting languages include UnixShell, AppleScript, CShell, and MSDOS batch files (see "Free On-Line Dictionary of Computing" FOLDOC at http://foldoc.doc.ic.ac.uk/foldoc). Furthermore, the cited design analyzer and database of problematic design elements of Fields-1 (FIG. 1, 106 and 108) in no apparent manner correspond to documentation of a design script. Therefore, the Office Action fails to show that Fields-1 anticipates claim 5.

Claim 6 in group VI includes limitations of entering documentation for simulation elements in a database and linking the documentation with associated ones of the simulation elements. The rejection relies on the database of problematic design elements of Fields-1 as corresponding to these limitations. However, this alleged correspondence fails to show that any database in Fields-1 includes either simulation elements or documentation related thereto. Therefore, claim 6 is not shown to be anticipated.

As to claims 7 and 8 in group VII, the rejection fails to show the limitations of inspecting the functional design elements and simulation elements for associated documentation; and reporting documentation deficiencies in association with the functional design elements and simulation design elements. The most recent rejection alleges that the teaching in Fields-1 of a database containing examples of coding styles found to be inefficient and subsequent queries to the database corresponds to these limitations. However, those skilled in the art will understand that documentation is not identical to examples of coding styles. More importantly, the rejection fails to recognize the limitations of inspecting design elements for the documentation versus inspecting a design element to see if it matches an entry in a database of problematic design elements. Therefore, claims 7 and 8 are not shown to be anticipated.

Without complete correspondence, the §102 rejection cannot stand. Accordingly, Appellants submit that the §102 rejection is improper and the rejection of claims 1-9, 14, and 16-19 must be overruled.

Claims 1, 9, 16, 17, 18, and 19 of group I are separately patentable over the claims in the other groups because the limitations of the claims in the other groups are not

necessarily present in the group I claims and the limitations of the group I claims are not taught by the prior art.

Claim 2 of group II is separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than group I) are not necessarily present in claim 2, and the limitations of translating the functional design elements into a netlist, and linking elements of the netlist with selected ones of the functional design elements are not necessarily present in the claims of the other groups (other than group III) nor are the limitations taught by the prior art.

Claims 3 and 14 of group III are separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than groups I and II) are not necessarily present in claims 3 and 14, and the limitation of linking elements of the physical implementation with selected ones of the functional design elements is not necessarily present in the claims of the other groups nor are the limitations taught by the prior art.

Claim 4 of group IV is separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than group I) are not necessarily present in claim 4, and the limitations of entering simulation elements in the database; and linking the simulation elements to associated ones of the design elements are not necessarily present in the claims of the other groups (other than groups V and VI) nor are the limitations taught by the prior art.

Claim 5 of group V is separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than groups I and IV) are not necessarily present in claim 5, and the limitations of

entering documentation for a design script in the database and linking the documentation of the design script to the design elements comprising the design module are not necessarily present in the claims of the other groups nor are the limitations taught by the prior art.

Claim 6 of group VI is separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than groups I and IV) are not necessarily present in claim 6, and the limitations of entering documentation for simulation elements in a database and linking the documentation with associated ones of the simulation elements are not necessarily present in the claims of the other groups nor are the limitations taught by the prior art.

Claims 7 and 8 of group VII are separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than groups I, IV, and VI) are not necessarily present in claims 7 and 8, and the limitations of inspecting the functional design elements and simulation elements for associated documentation and reporting documentation deficiencies in association with the functional design elements and simulation design elements are not necessarily present in the claims of the other groups nor are the limitations taught by the prior art.

Issue 2: The §103(a) rejection of claims 1, 9, 11, and 18-19 (groups I and VIII) is improper because the asserted *Gentry* and *Emacs* references fail to teach or suggest every limitation of the claims, the rejection fails to cite evidence of motivation, and there is no apparent likelihood of successfully combining the references.

In order to establish a *prima facie* case of obviousness, the asserted prior art references must teach or suggest all the claim limitations, evidence must be provided to support a motivation for modifying the reference to arrive at the claimed invention, and there must be a reasonable likelihood that the references could be successfully combined. The issued Office Actions fail to meet these requirements.

The rejection fails to show all the limitations of the independent claims 1, 18, and 19. For example, the rejection alleges that *Gentry* suggests the limitations of storing simulation results in the database and linking the simulation results with the functional design elements. However, the cited elements of *Gentry's* FIG. 2 and associated text only generally suggest simulation. There is no apparent mention of where or how the simulation results are stored, much less linking the results to specific functional design elements. Therefore, the rejection fails to show that all the limitations are suggested.

The final Office Action further cites *Gentry's* FIG. 2, items 36, 36', 40, and 42 as teaching these limitations. However, *Gentry's* accompanying description states:

> Any selected implementations of functions already stored in design infobase 36 or any functions designed during the design and verify phase 42 and their associated implementations are output to design infobase 36'. The design infobase 36' is then stored by database manager 34' for possible future analysis of the system

> described by the design infobase 36'. Also the database manager 34' stores any functions which were newly generated to complete design infobase 36'. By incorporating these newly generated functions as separate entities they become available for future system developments. Also following design and verify phase 42, the design engineer fabricates and bench tests the verified design, as shown at fabricate and bench test block 44. In this phase, the design engineer typically builds the system or a hardware model of the system and tests the system. The fabricate and bench test phase 44 provides a more approximate prototype than the modeling and testing performed at design and verify stage 42. If the design engineer is satisfied with the results during the fabricate and bench test phase 46, the development process then proceeds to hardware/software (HW/SW) integration phase 48. At HW/SW integration phase 48, the design engineer typically directs fabrication of a full working model of the system for final testing and possible production use. (col. 5, ll. 37-61).

No teaching in this text appears to teach the limitations of storing the simulation results in a database and linking the simulation results with the functional design elements. Instead, this text appears to suggest storing *various implementations* of functions in design infobases 36 and 36'. The text suggests simulation but does not address storage of the simulation results, in a database or elsewhere, nor any linking with functional design elements. Even though Appellants requested clarification, no further portions of *Gentry* were cited in support of the alleged teaching of the claim limitations.

Claim 9 depends from claim 1 and *prima facie* obviousness is not established for at least the reasons set forth above. Furthermore, those skilled in the art will appreciate that the limitations of inspecting for and reporting undesirable design characteristics are not suggested by *Emacs* reported VHDL compiler errors. A coding error detected by a compiler is a coding characteristic, not a characteristic of the design.

Claim 11 depends from claim 9 and includes limitations of inspecting the functional design elements for adherence to predefined design rules and reporting violations of the design rules. Those skilled in the art will recognize that design rules are not the same as proper VHDL syntax, nor are any design rules suggested by VHDL syntax.

The alleged motivation for combining *Emacs* with *Gentry* is conclusory and therefore, improper. Furthermore, no evidence is provided from the prior art to suggest the combination, and no evidence is provided to show a likelihood of successfully combining the references. Therefore, for these reasons and because the rejection fails to show a suggestion of all the limitations, *prima facie* obviousness is not established.

The alleged motivation for modifying *Gentry* with *Emacs* is that "the use of a VHDL compiler to test for errors is integral to the use of VHDL." However, there is no evidence cited from *Gentry* to suggest an additional need to further provide VHDL processing. Nor is there any evidence that Gentry's system is prone to the problems allegedly addressed by *Emacs*. Addressing the "rigorous … requirement for a showing of the teaching or motivation to combine prior art references," the Court of Appeals for the Federal Circuit has stated:

> We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, (citations omitted), although "the suggestion more often comes from the teachings of the pertinent references," *Rouffet*, 149 F.3d at 1355, 47 USPQ2d at 1456. The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. *See, e.g., C.R. Bard*, 157 F.3d at 1352, 48 USPQ2d at 1232. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not

"evidence." (citation omitted) *In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

The alleged motivation is merely a broad conclusory statement of a general function of a VHDL compiler. The alleged motivation lacks clear and particular reasons that would lead one of ordinary skill in the art to modify specific teachings of *Gentry* with those of *Emacs*.

For at least these reasons, the rejection fails to establish a *prima facie* case of obviousness for the claims in groups I and VIII. Accordingly, Appellants submit that the §103 rejection is improper and the rejection must be withdrawn.

Claim 9 of group I is separately patentable over the other claims in group I because the limitations of inspecting for and reporting undesirable design characteristics in claim 9 are not necessarily present in the claims 1, 18 and 19.

Claim 11 of group VIII is separately patentable over the claims in the other groups because the limitations of the claims in the other groups (other than group I) are not necessarily present in claim 11, and the limitations of inspecting the functional design elements for adherence to predefined design rules and reporting violations of the design rules are not necessarily present in the claims of the other groups nor are the limitations taught by the prior art.

Issue 3: The §103(a) rejection of claims 2-3 and 14 is improper because the asserted *Gentry*, *Emacs*, and *XACT* references fail to teach or suggest every limitation of the claims, the rejection fails to cite evidence of motivation, and there is no apparent likelihood of successfully combining the references.

The issued Office Actions fail to establish a *prima facie* case of obviousness because the rejection does not establish that the asserted prior art references teach or suggest all the claim limitations, does not provide evidence to support a motivation for modifying the *Gentry-Emacs* combination with *XACT* to arrive at the claimed invention, and does not establish a reasonable likelihood that the references could be successfully combined.

Claims 2 and 14 depend from claim 1, and claim 3 depends from claim 2. As explained above, the rejection fails to establish a *prima facie* case of obviousness of claim 1 in view of the *Gentry-Emacs* combination. Therefore, for at least those reasons, *prima facie* obviousness is not established for claims 2, 3, and 14.

Furthermore, the rejection fails to provide sufficient motivation to modify the *Gentry-Emacs* combination with *XACT*. The alleged motivation is that it would have been obvious to do so in order to "create a VHD or VER file that can be simulated for back annotation within Synopsys", which would "enable keeping both versions updated whenever changes were made in one of the files." This motivation is improper because it is no more than a general statement of functions from the individual references.

The Office Action fails to provide evidence of a suggestion of all the limitations of the pending claims, fails to provide a proper motivation for modifying the teachings of

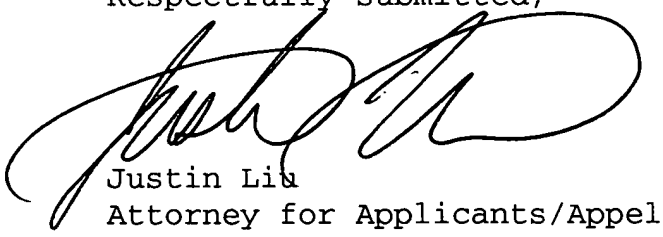
Gentry with *Emacs* and *XACT*, and fails to provide evidence of a reasonable likelihood of success in modifying the teachings of Gentry with Emacs and XACT. Therefore, a *prima facie* case of obviousness has not been established, and the rejection should be withdrawn. This motivation lacks the requisite clear and particular reasons that would lead one of ordinary skill in the art to modify specific teachings of *Gentry* and *Emacs* with specific teachings of *XACT*.

Claim 2 of group II and claims 3 and 14 of group III are separately patentable over the claims in the other groups for the reasons set forth above under Issue 1.

IX. Conclusion

In view of the above, Appellants believe the claimed invention to be patentable. Claims 1-19 remain for consideration. Appellants respectfully request reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Respectfully submitted,



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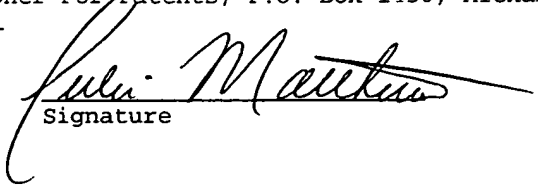
Julie Matthews
Name



Signature

APPENDIX OF APPEALED CLAIMS (09/510,203)

1. A computer-implemented method for developing a reusable electronic circuit design module, wherein the design module is comprised of one or more functional design elements comprising the design module, comprising:

entering the functional design elements into a database;

entering documentation elements into the database;

linking the functional design elements with selected ones of the documentation elements;

simulating a testbench with the design module, whereby simulation results are generated;

storing the simulation results in the database; and

linking the simulation results with the functional design elements.

2. The method of claim 1, further comprising:

translating the functional design elements into a netlist; and

linking elements of the netlist with selected ones of the functional design elements.

3. The method of claim 2, further comprising:

translating the functional design elements into a physical implementation; and

linking elements of the physical implementation with selected ones of the functional design elements.

4. The method of claim 1, further comprising:

entering simulation elements in the database; and

linking the simulation elements to associated ones of the design elements.

5. The method of claim 4, further comprising:

entering documentation for a design script in the database; and

linking the documentation of the design script to the design elements comprising the design module.

6. The method of claim 4, further comprising:

entering documentation for the simulation elements in the database; and

linking the documentation for the simulation elements with associated ones of the simulation elements.

7. The method of claim 6, further comprising:

inspecting the functional design elements and simulation elements for associated documentation; and

reporting documentation deficiencies in association with the functional design elements and simulation design elements.

8. The method of claim 1, further comprising:

inspecting the functional design elements for associated documentation; and

reporting documentation deficiencies in association with the functional design elements.

9. The method of claim 1, further comprising:

inspecting the functional design elements for undesirable design characteristics; and

reporting the undesirable design characteristics found in the functional design elements.

10. The method of claim 9, further comprising:

inspecting the functional design elements for undesirable hierarchical characteristics; and

reporting discovered ones of the undesirable hierarchical characteristics.

11. The method of claim 9, further comprising:

inspecting the functional design elements for adherence to predefined design rules; and

reporting violations of the design rules.

12. The method of claim 11, further comprising providing assistance in specifying the design rules for the functional design elements.

13. The method of claim 9, further comprising:

monitoring changes made to the functional design elements; and

indicating which of the functional design elements are dependent on the changes.

14. The method of claim 1, further comprising:

translating the functional design elements into a physical implementation; and

linking elements of the physical implementation with selected ones of the functional design elements.

15. The method of claim 1, further comprising requiring specification of parameters at a top level of a hierarchy of the design module.

16. The method of claim 1, further comprising displaying the functional design elements linked to errors in the simulation results.

17. The method of claim 16, further comprising displaying documentation elements associated with errors in the simulation results.

18. An apparatus for developing a reusable electronic circuit design module, wherein the design module is comprised of one or more functional design elements comprising the design module, comprising:

means for entering the functional design elements into a database;

means for entering documentation elements into the database;

means for linking the functional design elements with selected ones of the documentation elements;

means for simulating a testbench with the design module, whereby simulation results are generated;

means for storing the simulation results in the database; and

means for linking the simulation results with the functional design elements.

19. A system for developing a reusable electronic circuit design module, wherein the design module is comprised of one or more functional design elements comprising the design module, comprising:

a database arranged for storage of the design elements and documentation elements;

a design inspector coupled to the database, the design inspector configured and arranged to link the functional design elements with selected ones of the documentation elements;

a debugging-support module coupled to the simulator and to the database, the debugging-support module configured and arranged to generate a netlist from the design module, wherein the netlist is suitable for simulation;

a functional simulator coupled to the debugging-support module, the simulator configured and arranged to simulate a testbench with the design module, whereby simulation results are generated; and

wherein the debugging-support module is further configured and arranged to store the simulation results in the database and link the simulation results with the functional design elements.